CCD231-42 Back Illuminated Scientific CCD Sensor 2048 x 2064 Pixels, Four Outputs

INTRODUCTION

This device extends e2v's family of scientific CCD sensors. The CCD231 has been designed to provide a large image area for demanding scientific imaging applications. Back-illuminated spectral response combined with low read-out noise give exceptional sensitivity. The device has been designed for applications such as low-noise spectroscopy and broadband imaging.

DESCRIPTION

The sensor has an image area having 2048 x 2064 pixels, split readout registers at both top and bottom with charge detection amplifiers at both ends. The pixel size is 15 µm square. The image area has four separately connected sections to allow full-frame, frame transfer, split full frame or split frame-transfer modes. Depending on the mode, the readout can be through 1, 2 or 4 of the output circuits. A gate-controlled drain is also provided to allow fast dumping of unwanted data.

The output amplifier is a two-stage type designed to give minimum noise at pixel rates up to 3 MHz. The low output impedance of 400 Ω simplifies the interface with external electronics. Optional dummy outputs are also available to facilitate common mode rejection.

This preliminary data sheet relates to the back-illuminated version of the device. Other variants are available.

Specifications are guaranteed and tested at -100C.

OTHER VARIANTS

Alternate AR-coatings and inverted-mode options (IMO) can be provided. Devices with other formats (e.g. 4096 x 4096, 6144 x 6144, 8192 x 3172 pixels) or 4-side butting (metal/flexi package) can also be provided. Consult e2v technologies for further information.

A version (CCD230) is also available with lower responsivity output (3µV/e) offering larger charge handling capacity and a slightly higher maximum operating frequency.

Standard silicon and deep depletion silicon (better red response) can be provided. Consult e2v technologies for further information on all variants.

SUMMARY SPECIFICATION

Number of pixels	2048(H) x 2064(V)
Pixel size	15 µm square
Image area	30.7 mm x 31.0 mm
Outputs	4
Package size	33.3 x 61.0 mm
Package format	Alumina PGA
Focal plane height, above base	2.75 mm
Connectors	Pin Grid Array (PGA)
Flatness	<20 µm (peak to valley)
Amplifier sensitivity	7 µV/e^-
Readout noise	5 e^- at 1 MHz 2.5 e^- at 50 kHz
Maximum data rate	3 MHz
Pixel Charge storage	300,000 e^-
Dark signal	3 e^-/pixel/hour (at –100 °C)

Quoted performance parameters given here are "typical" values. Specification limits are shown later in this data sheet.

Part References

CCD231-42-g-xxx
G= cosmetic grade
xxx= specific part variant.
See below or consult e2v

CCD231-42-g-E71 standard silicon astro midband

CCD231-42-g-F61 deep depletion astro multi-2

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PERFORMANCE (At 173 K unless stated)

Electro-Optical Specification (CCD231 Normal Mode, see note 1)

	Min	Typical	Max	Units	Note
Peak charge storage (image)		350,000	-	e^-/pixel	2(a)
Peak charge storage (register/SW): OG low (mode 1) OG high (mode 2)	 - -	 300,000 350,000	 	 e^-/pixel e^-/pixel	2(b)
Output node capacity: OG low (mode 1) OG high (mode 2)	 200,000 -	 300,000 600,000	 - -	 e^- e^-	2(c)
Output amplifier responsivity: mode 1 mode 2	 5.0 -	 7.0 2.5	 - -	 $\mu V/e^-$ $\mu V/e^-$	3
Readout noise	-	2.5	4	e^- rms	4
Maximum readout frequency	-	1000	3000	kHz	5
Dark signal: at 173 K at 153 K	 - -	 3 0.02	 - 2.0	 e^-/pixel/hr e^-/pixel/hr	6
Charge transfer efficiency: parallel serial	 99.9990 99.9990	 99.9995 99.9995	 100 100	 % %	7
Spectral range	300	-	1060	nm	
Peak quantum efficiency	-	90	-	%	

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency of approximately 0.1 – 1.0 MHz. The noise as specified is separately measured in accordance with note 4.
2. (a) Signal level at which resolution begins to degrade. Device is non-inverted (NIMO/non-MPP), for maximum full well. This value is not factory tested, since this is only possible in mode-2; factory tests do not include mode-2 operation.

   (b) The summing well capacity limits the charge in the register, and its value varies with mode as shown. Not factory tested.

   (c) The signal handled by the output node (for linear operation) varies with mode as shown. Only mode-1 is tested.

   Only one charge capacity test is performed, in mode-1, with no binning. The output node therefore is expected to be the limiting capacity.
3. Under normal operation (mode 1), SW is operated as a summing well or clocked as R∅3. OG is biased at a low DC level. Note: in this mode (with lowest read noise) the output cannot handle the full available pixel charge capacity.

   Alternatively (mode 2), SW may be operated as an output gate (and not therefore available for summing), biased at a low DC level, with OG raised to a high voltage (see note 9). This gives more charge-handling capacity (e.g. for higher level pixel binning) but may have poorer linearity than mode-1. Charge transfer to the output now occurs as R∅2 goes low. In mode-2, the output noise will also increase by a factor of three. Mode-2 is not factory tested.
4. Measured with correlated double sampling at 50 kHz nominal (mode 1). e2v test camera uses clamp & sample CDS.
5. Depending on the external load capacitance to be driven. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.
6. Dark signal is typically measured at a device temperature of 173 K. It is a strong function of temperature and the typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K is given by:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

   Note that this is typical performance and some variation may be seen between devices. Dark current is lowest with the substrate voltage at +9 V, and somewhat higher with substrate at 0 V.
7. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Grade	0	1	2
Column defects, black or white	0	2	10
White spots	100	150	300
Total (black & white) spots	100	300	500
Traps > 200e-	5	10	20

Grade 5 devices are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

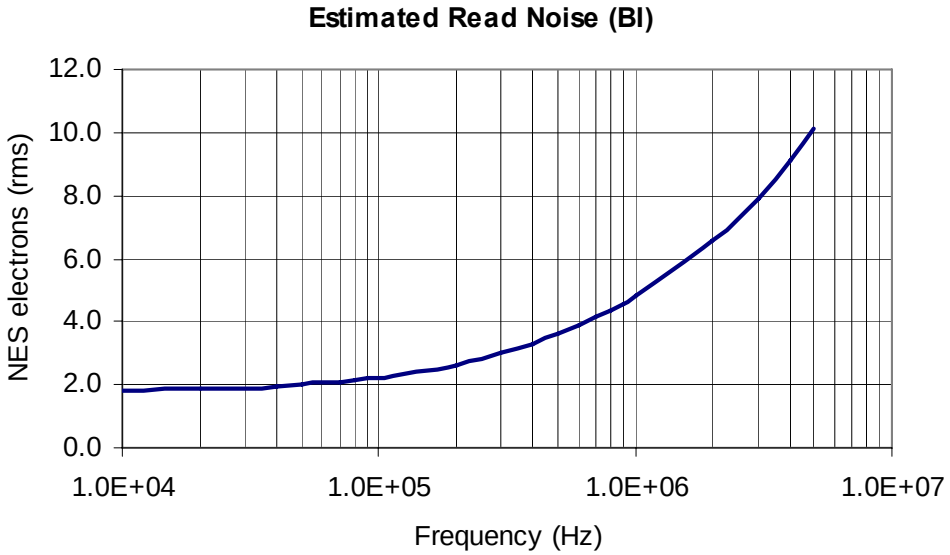
DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is ≥ 5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 6 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^-
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

TYPICAL OUTPUT AMPLIFIER NOISE

The variation of typical read noise with operating frequency is shown below. (Measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1 at approximately 173 K).

Note. This curve indicates anticipated performance using a dual slope integration CDS system. The noise, as specified in the previous performance table is measured with the e2v test camera which uses a clamp and sample CDS system (which delivers slightly higher read-noise).



SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants.

Standard silicon devices

	Standard silicon Astro Broadband	Standard silicon Astro Midband	Standard silicon Astro Multi-2	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	30	-
400	70	50	75	3
500	80	80	75	-
650	75	80	80	3
900	25	25	25	5

Deep depletion devices

	Deep depletion silicon Astro Broadband	Deep depletion silicon Astro Midband	Deep depletion silicon Astro ER1 response	Deep depletion silicon Astro Multi-2	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	20	30	-
400	70	50	35	75	3
500	75	80	65	75	-
650	70	80	80	80	3
900	40	40	45	50	5

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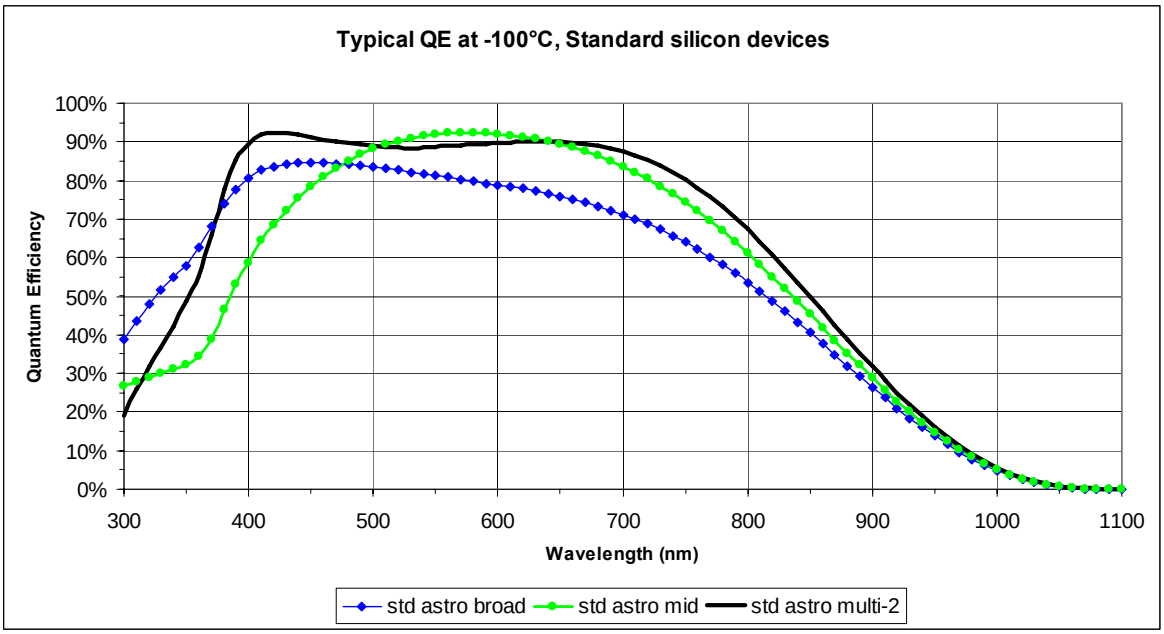
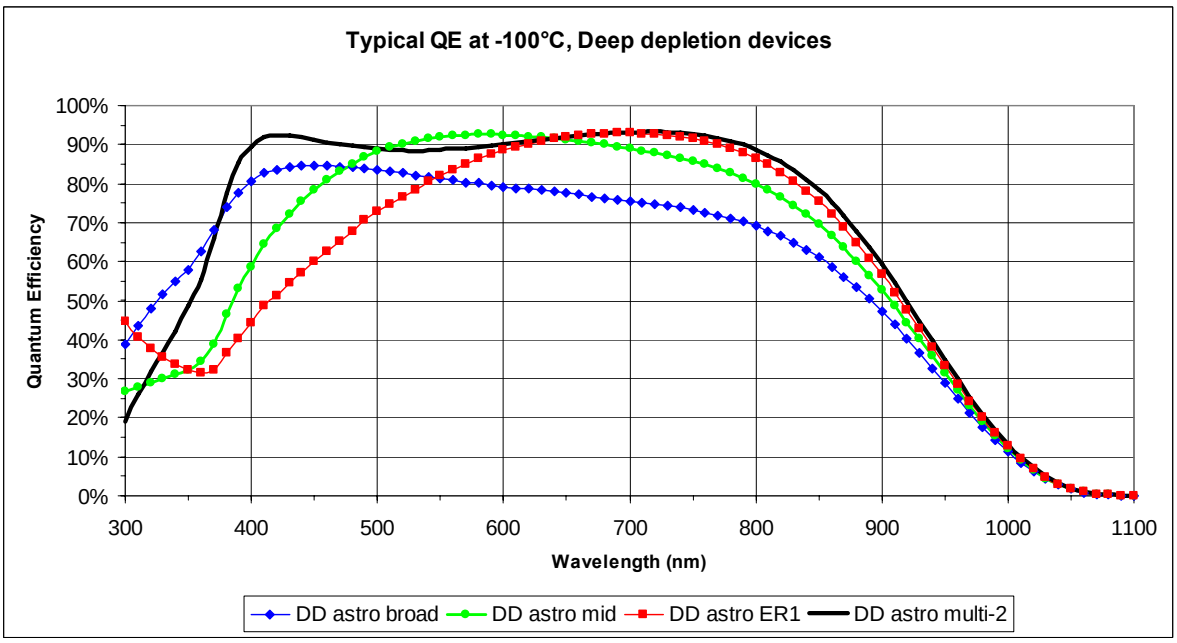
Notes

The multi-AR coatings are currently considered as pre-production types prior to full process release.
The multi-2 coating is designed for wide-range use.

Currently only some of the above coatings are available. Devices with an alternate spectral response may be available. Consult e2v technologies.

See also the figures below.


Typical QE at -100°C, Standard silicon devices
Quantum Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)
std astro broad
std astro mid
std astro multi-2


Typical QE at -100°C, Deep depletion devices
Quantum Efficiency
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
300
400
500
600
700
800
900
1000
1100
Wavelength (nm)
DD astro broad
DD astro mid
DD astro ER1
DD astro multi-2

DEFINITIONS

Back-Thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is “passivated” and an anti-reflection coating may be added.

AR coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infrared regions. For X-ray detection an uncoated device may be preferable.

Inverted Mode (IMO)

An inverted mode CCD has an additional implant that allows charge integration to be carried out with all clock phases low. With a high voltage applied to the substrate (typically +9 V) this causes the whole of the device to be flooded with holes (inverted or pinned), which suppresses the surface component of dark signal. This leaves only the much lower bulk component, reducing the overall dark signal by a factor of approximately 100.

Inverted mode operation is also referred to as multi-phase pinning (MPP).

Readout Noise

Readout noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy Output

Each output has an associated “dummy” circuit on-chip, which is of identical design to the “real” circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the “real” signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down.

Dark Signal

This is the output signal of the device with zero illumination. This typically consists of thermally generated electrons within the semiconductor material, which are accumulated during signal integration. Dark signal is a strong function of temperature as described in note 6.

Correlated Double Sampling

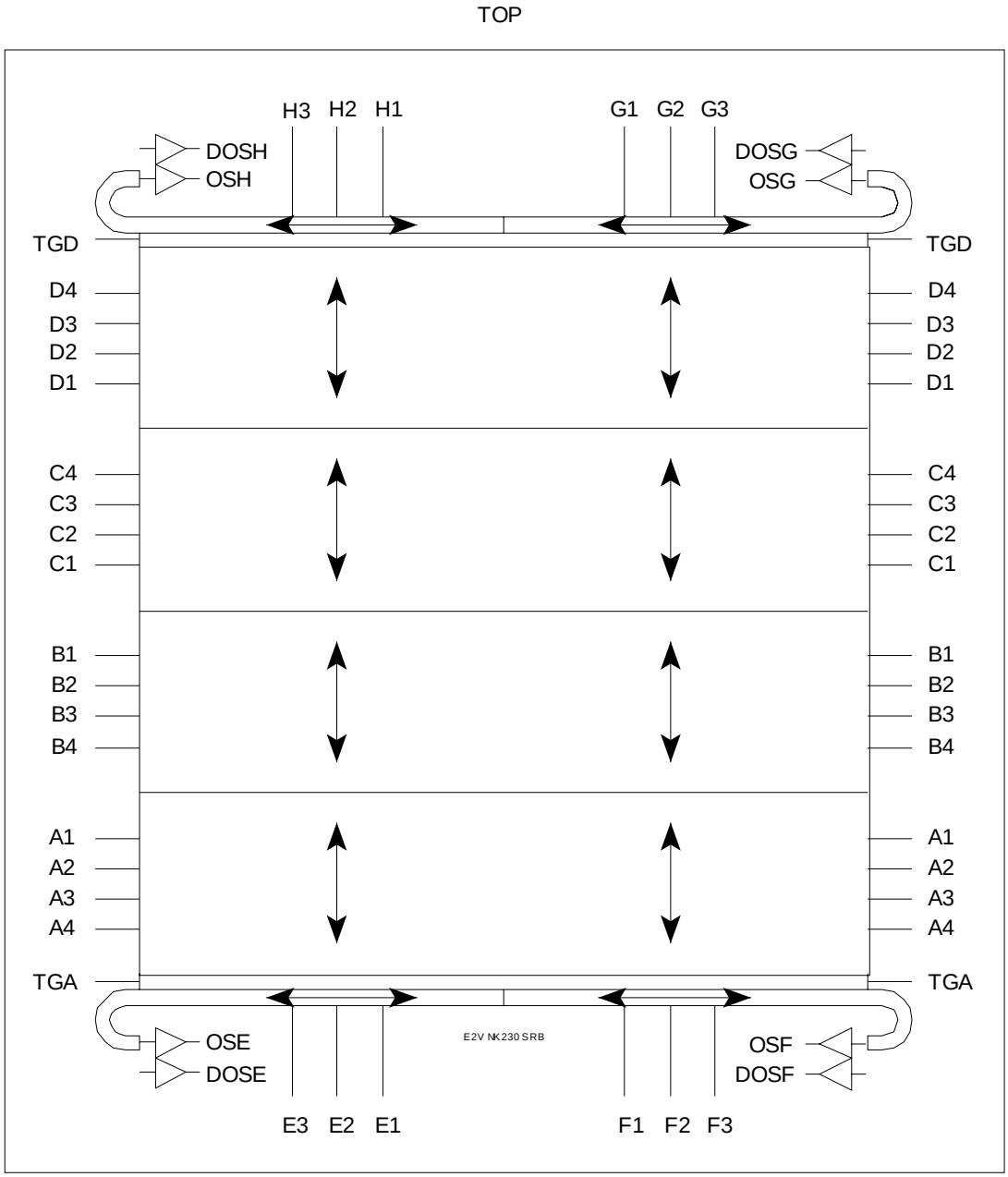
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

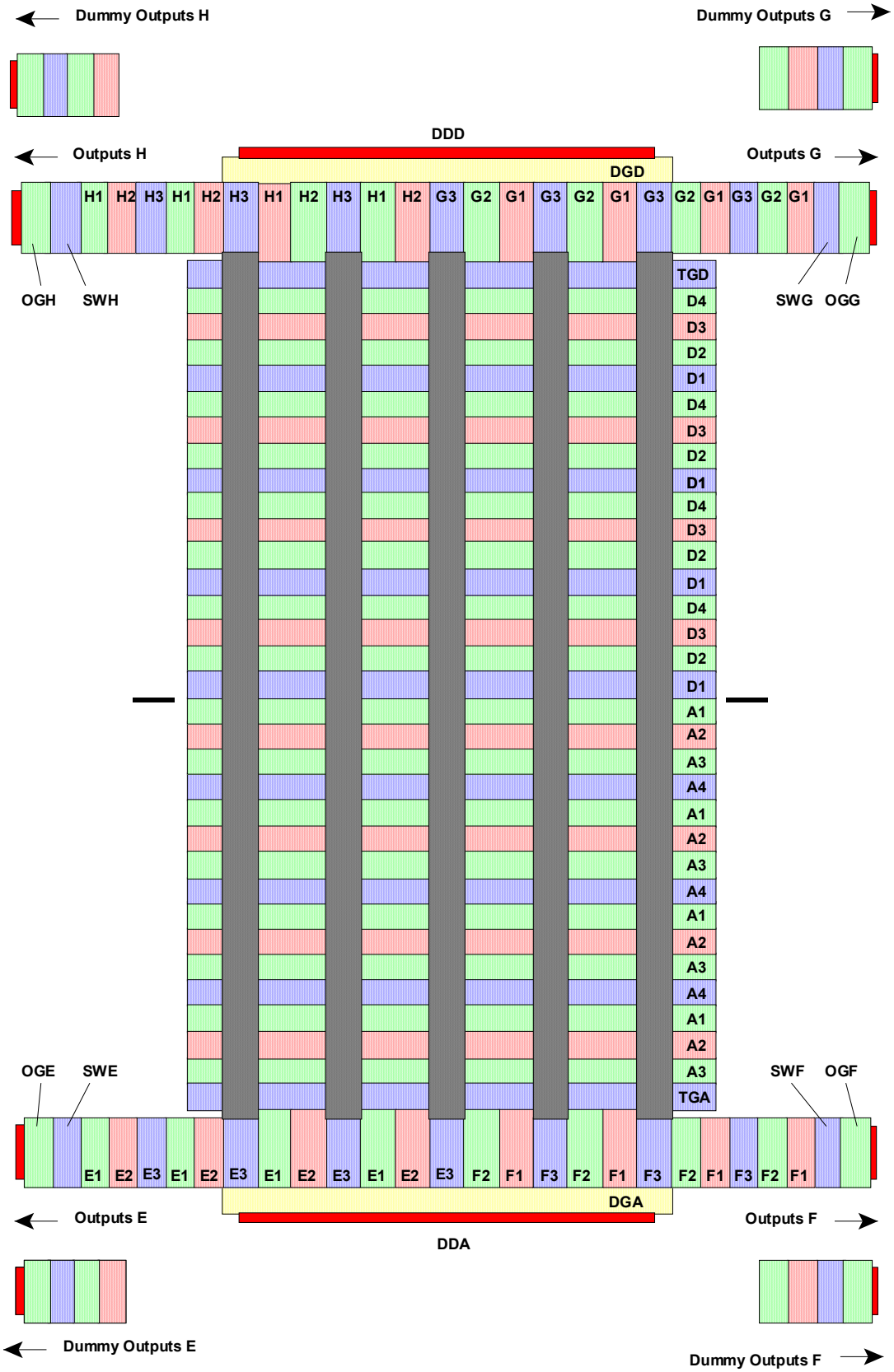
ARCHITECTURE

Chip Schematic



Sections B & C have 512 rows each. Sections A & D have 520 rows each.
Each row has 2048 image elements.

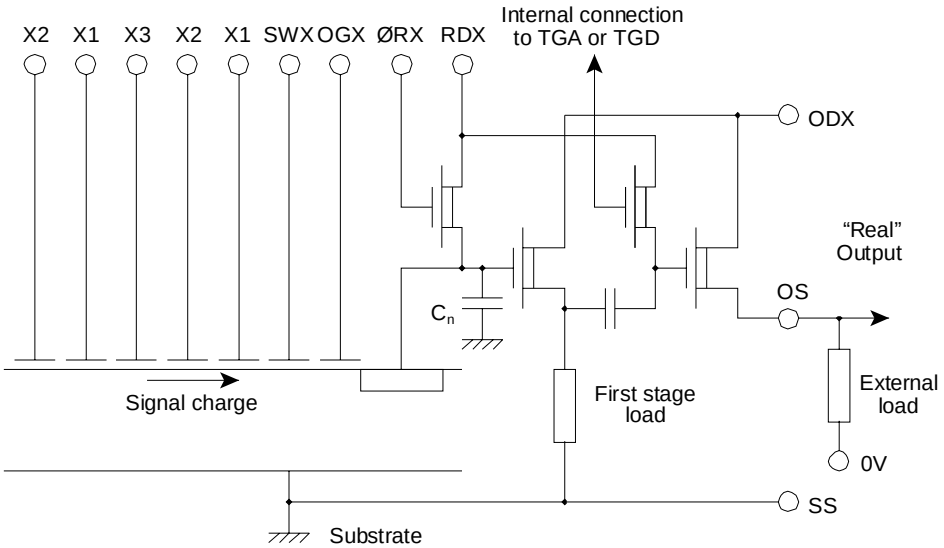
ARRANGEMENT OF ELECTRODES

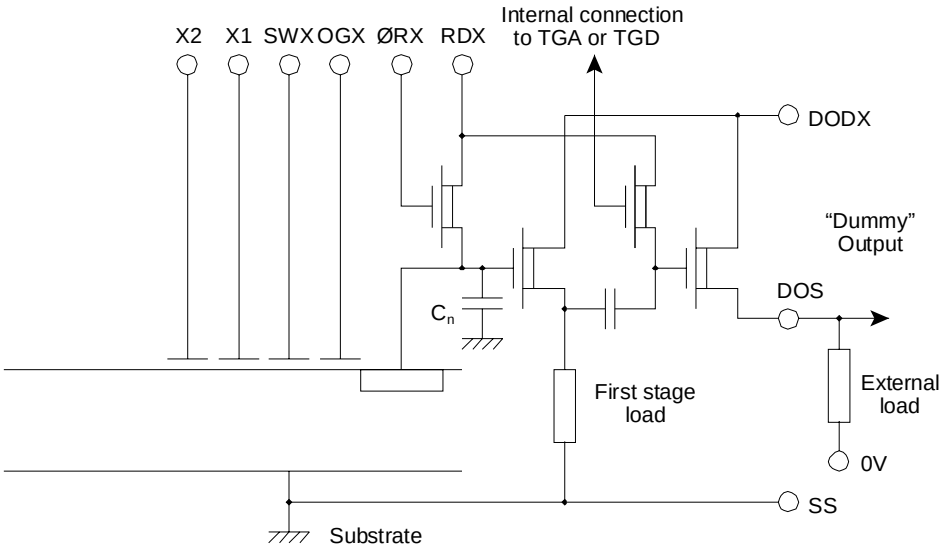


OUTPUT CIRCUIT

X designates a specific output, namely E, F, G or H

The ‘mapping table’ on p14 shows the relationship between serial drive phases (RØ1,etc) and device clock pins (X1, X2 etc)





The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.3 mA.

The output circuit consists of two capacitor-coupled source-follower stages. This particular design has a reduced responsivity to allow binning of large charge packets. The load for the first stage is on-chip and that for the second stage is external, as next described. The DC restoration circuitry requires a pulse at the start of line readout, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry. N.B. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

If an output is to be powered down, it is recommended that either OD or DOD be set to SS voltage, taking care that the maximum ratings are never exceeded or that OD and DOD be disconnected. If external loads return to a voltage below SS they should also be disconnected.

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

The tables below give the pin-outs and clock amplitudes. Note that the hyphenated suffix symbols (e.g. ∅R-H) indicate to which amplifier the CCD pin relates.

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 10)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	B2	Image Area Clock Phase 2 (B)	9	10	12	±20
2	B1	Image Area Clock Phase 1 (B)	9	10	12	±20
3	B3	Image Area Clock Phase 3 (B)	9	10	12	±20
4	B4	Image Area Clock Phase 4 (B)	9	10	12	±20
5	DOD-E	Dummy Output Drain (E)	25	27.5	31	-0.3 to +35
6	TG-A	Transfer Gate (A)	9	10	12	±20
7	ØR-E	Reset Gate (E)	9	12	14	±20
8	RD-E	Reset Drain (E)	16	17	19	-0.3 to +25
9	DOS-E	Dummy Output Source (E)		See note 8		N/A
10	SS	Substrate (see note 15)	0	0	10	N/A
11	OD-E	Output Drain (E)	25	27.5	31	-0.3 to +35
12	OS-E	Output Source (E)		See note 8		N/A
13	SS	Substrate (see note 15)	0	0	10	N/A
14	OG-E	Output Gate (E) (see note 9)	1	2.5	(note 9)	±20
15	N/C	No Connection		-		N/A
16	E2	Register Clock Phase 2 (E)	9	10	12	±20
17	E1	Register Clock Phase 1 (E)	9	10	12	±20
18	SWØ-E	Summing Well (E) (see note 9)	9	10	12	±20
19	DG-A	Dump Gate (A) (see note 11)	-2	0	0.5	±20
20	DD-A	Dump Drain (A)	24	29	31	-0.3 to +35
21	E3, F3	Register Clock Phase 3 (F and E)	9	10	12	±20
22	F1	Register Clock Phase 1 (F)	9	10	12	±20
23	F2	Register Clock Phase 2 (F)	9	10	12	±20
24	SWØ-F	Summing Well (F) (see note 9)	9	10	12	±20
25	SS	Substrate (see note 15)	0	0	10	N/A
26	OG-F	Output Gate (F) (see note 9)	1	2.5	(note 9)	±20
27	N/C	No Connection		-		N/A
28	SS	Substrate (see note 15)	0	0	10	N/A
29	OD-F	Output Drain (F)	25	27.5	31	-0.3 to +35
30	OS-F	Output Source (F)		See note 8		N/A
31	ØR-F	Reset Gate (F)	9	12	14	±20
32	RD-F	Reset Drain (F)	16	17	19	-0.3 to +25
33	DOS-F	Dummy Output Source (F)		See note 8		N/A
34	A4	Image Area Clock Phase 4 (A)	9	10	12	±20
35	DOD-F	Dummy Output Drain (F)	25	27.5	31	-0.3 to +35
36	TG-A	Transfer Gate (A)	9	10	12	±20
37	A2	Image Area Clock Phase 2 (A)	9	10	12	±20
38	A1	Image Area Clock Phase 1 (A)	9	10	12	±20
39	A3	Image Area Clock Phase 3 (A)	9	10	12	±20

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 10)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
40	C3	Image Area Clock Phase 3 (C)	9	10	12	±20
41	C4	Image Area Clock Phase 4 (C)	9	10	12	±20
42	C2	Image Area Clock Phase 2 (C)	9	10	12	±20
43	C1	Image Area Clock Phase 1 (C)	9	10	12	±20
44	DOD-G	Dummy Output Drain (G)	25	27.5	31	-0.3 to +35
45	TG-D	Transfer Gate (D)	9	10	12	±20
46	ØR-G	Reset Gate (G)	9	12	14	±20
47	RD-G	Reset Drain (G)	16	17	19	-0.3 to +25
48	DOS-G	Dummy Output Source (G)		See note 8		N/A
49	SS	Substrate (see note 15)	0	0	10	N/A
50	OD-G	Output Drain (G)	25	27.5	31	-0.3 to +35
51	OS-G	Output Source (G)		See note 8		N/A
52	SS	Substrate (see note 15)	0	0	10	N/A
53	OG-G	Output Gate (G) (see note 9)	1	2.5	(note 9)	±20
54	N/C	No Connection		-		N/A
55	G2	Register Clock Phase 2 (G)	9	10	12	±20
56	G1	Register Clock Phase 1 (G)	9	10	12	±20
57	SWØ-G	Summing Well (G) (see note 9)	9	10	12	±20
58	DG-D	Dump Gate (D) (see note 11)	-2	0	0.5	±20
59	DD-D	Dump Drain (D)	24	29	31	-0.3 to +35
60	G3, H3	Register Clock Phase 3 (G and H)	9	10	12	±20
61	H1	Register Clock Phase 1 (H)	9	10	12	±20
62	H2	Register Clock Phase 2 (H)	9	10	12	±20
63	SWØ-H	Summing Well (H) (see 0)	9	10	12	±20
64	SS	Substrate (see note 15)	0	0	10	N/A
65	OG-H	Output Gate (H) (see 0)	1	2.5	(note 9)	±20
66	N/C	No Connection		-		N/A
67	SS	Substrate (see note 15)	0	0	10	N/A
68	OD-H	Output Drain (H)	25	27.5	31	-0.3 to +35
69	OS-H	Output Source (H)		See note 8		N/A
70	ØR-H	Reset Gate (H)	9	12	14	±20
71	RD-H	Reset Drain (H)	16	17	19	-0.3 to +25
72	DOS-H	Dummy Output Source (H)		See note 8		N/A
73	D1	Image Area Clock Phase 1 (D)	9	10	12	±20
74	DOD-H	Dummy Output Drain (H)	25	27.5	31	-0.3 to +35
75	TG-D	Transfer Gate (D)	9	10	12	±20
76	D3	Image Area Clock Phase 3 (D)	9	10	12	±20
77	D4	Image Area Clock Phase 4 (D)	9	10	12	±20
78	D2	Image Area Clock Phase 2 (D)	9	10	12	±20

See Notes Overleaf

NOTES

8. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is then about 6 - 8 V above the reset drain voltage and is typically 24 V. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

   For highest speed operation the output load resistor can be reduced from 5 kΩ to approximately 2.2 kΩ, but note that this will increase power consumption. If the device is to be operated with a register clock period of below about 1 MHz then the load may be increased to 10 kΩ to reduce power consumption.

9. Default operation (mode 1) shown with OG at +2 V typical. In this mode SW may be clocked as R∅3 if a summing well function is not required. OG-Lo should have a maximum value of +5V.

   For alternative operation in a low responsivity mode (mode 2) with increased charge handling, OG should be set to OG-Hi and SW should be operated as OG-Lo (i.e. 2V typical). See below for appropriate OG-Hi values. Charge is now read out as R∅2 goes low.

   See note 12 also for discussion about Substrate voltage (Vss). With high substrate voltage OG-Hi may be set to a nominal +20V, which offers best linearity in mode-2. With low substrate voltage the allowed maximum value of OG-Hi is limited to a nominal +18V; the lower OG-Hi value has a greater non-linearity.

10. To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0 V).

    The clock pulse low levels should be in the range 0 ± 0.5 V for image, register, SW and DG clocks. The register and SW clock low level should be +1 V higher. Reset clock low may be nominally 0 V or +1 V.

    In all cases, specific recommended settings will be supplied with each science-grade sensor.

11. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V (this may be provided from a common rail to the register clocks). The Dump Gate operation is not factory tested at e2v.

12. This data sheet assumes that all signals are relative to the clock low level of 0 V .The absolute level for all biases and clock rails may be changed to suit the needs of the designer provided the relative levels are maintained. For example, it is acceptable to set Vss to 0 V so long as the specified difference between Vss and all other bias and clock voltages is maintained and the current load on all output sources is as recommended in note 8.

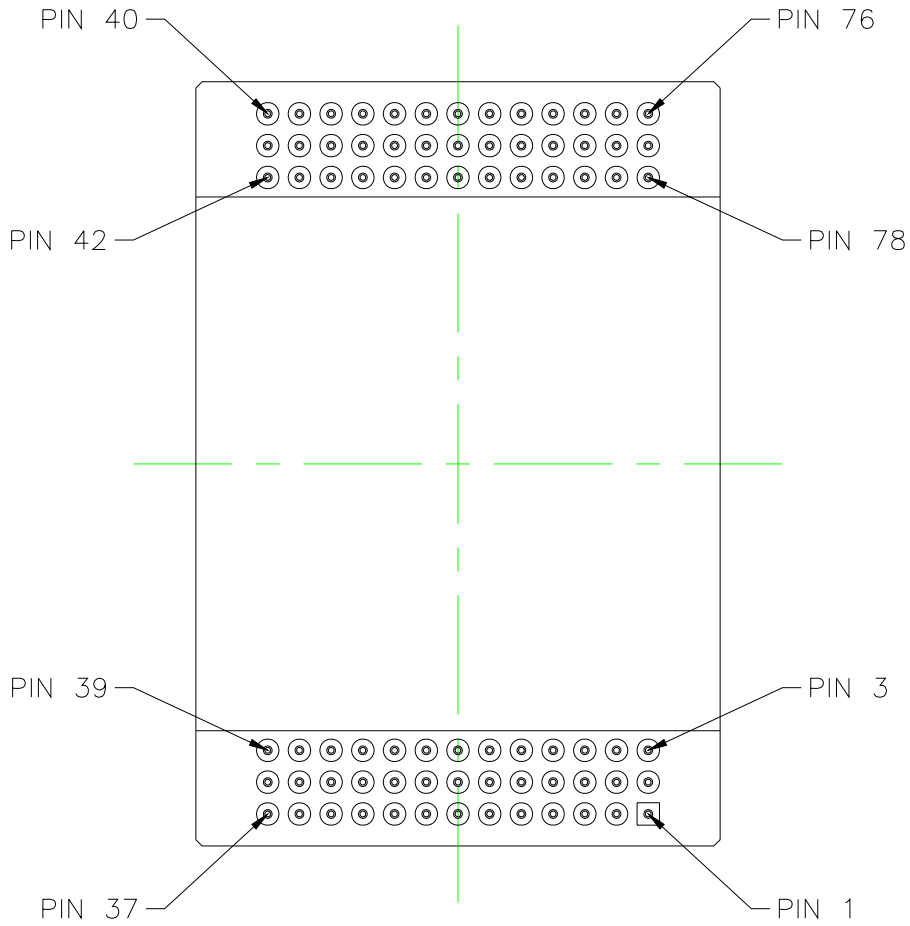
13. DD and OD may be provided from a common rail provided that they are separately filtered sufficiently to ensure that there is no clock pick-up on OD.

14. Image and register clock high voltages may be provided from common rails.

15. The substrate voltage (Vss) has a default recommended value of 0V (“low” substrate). This is particularly recommended for deep-depletion device variants, since it optimises depletion depth for best Point Spread Function. Devices may alternatively be operated at “high” substrate, with Vss=9V. The high substrate setting offers slightly lower dark current, although this is usually not of primary concern when the device is cryogenically cooled.
    The substrate setting has some consequence for the allowed OG upper voltage level, as discussed in note 9.

PIN CONNECTIONS

VIEW FACING UNDERSIDE OF PACKAGE



ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
I∅/I∅ inter-phase [A, B, C and D]	2.5	nF
I∅/SS (A, B, C, D)	5	nF
Transfer gates [TGA, TGD]	65	pF
R∅/(SS + DG + DD) [E1, F1, G1, H1]	95	pF
R∅/(SS + DG + DD) [E2, F2, G2, H2]	90	pF
R∅/(SS + DG + DD) [E3, F3, G3, H3]	80	pF

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate. For example, the total capacitance on phase A1 is 2 times 2.5 nF plus 5 nF for a total of 10 nF.

The amplifier output impedance is typically 400 Ω.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltage for the amplifier and dump drains (pins 5, 8, 11, 20, 29, 32, 35, 44, 47, 50, 59, 68, 71 and 74) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 8) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

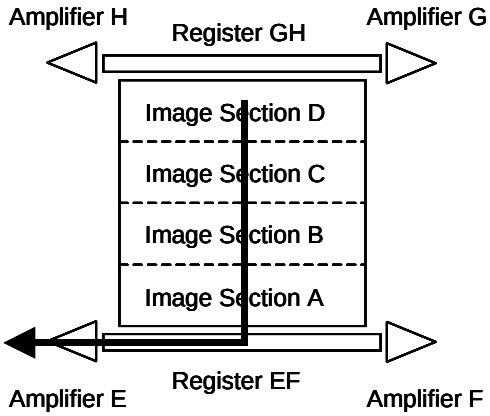
The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line read-out using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

Readout frequency	Line time	Amplifier load	Power dissipation			
			Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	11 ms	10 kΩ	165 mW	9 mW	2 mW	176 mW
1 MHz	1.1 ms	5 kΩ	275 mW	85 mW	17 mW	377 mW
3 MHz	400 µs	2.2 kΩ	525 mW	300 mW	50 mW	875 mW

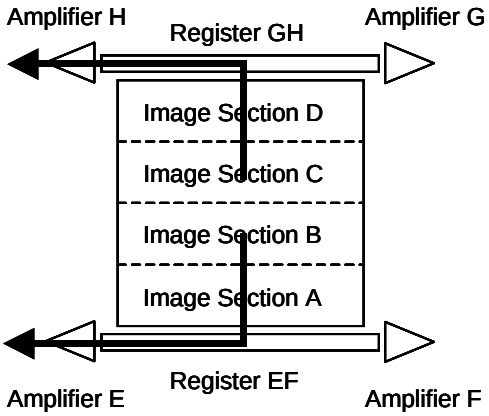
The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

FRAME READOUT MODES

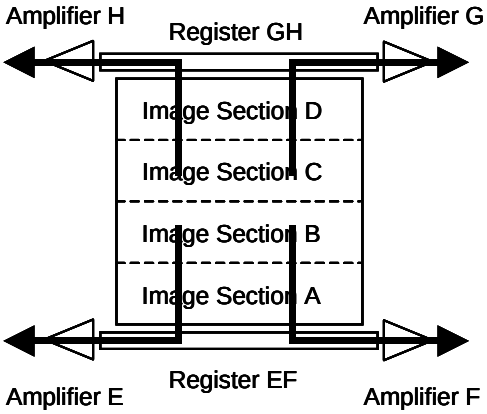
The device can be operated in a full-frame or frame transfer mode with readout from one, two or four amplifiers. These modes are determined by the clock pulse sequences applied to the image and register clocks. The diagrams below show some of the transfer options that are possible.



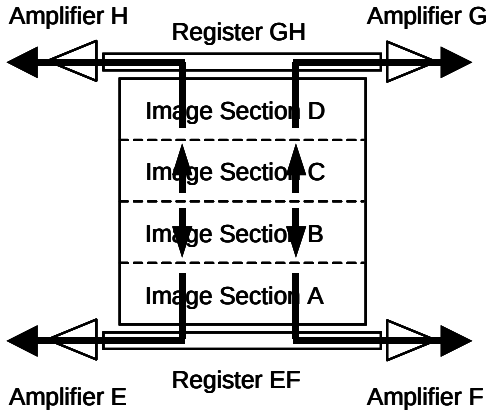
Full frame read-out through one amplifier



Split full frame read-out through two amplifiers



Split full frame read-out through four amplifiers



Split frame transfer through four amplifiers

If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

	IØ1	IØ2	IØ3	IØ4	
A section transfer towards E-F register	A4	A1	A2	A3	TGA = IØ1
B section transfer towards E-F register	B4	B1	B2	B3	
C section transfer towards G-H register	C1	C2	C3	C4	
D section transfer towards G-H register	D1	D2	D3	D4	TGD = IØ1
A section transfer towards G-H register	A4	A3	A2	A1	TGA = “low”
B section transfer towards G-H register	B4	B3	B2	B1	
C section transfer towards E-F register	C1	C4	C3	C2	
D section transfer towards E-F register	D1	D4	D3	D2	TGD = “low”

The first four transfer sequences are for split full-frame readout. The second four are for reversing the transfer direction in either section for readout to only one of the registers.

Transfer from the image section to the register is into the phase 1 and 2 electrodes, i.e. E1, F1, G1, H1, E2, F2, G2 and H2. These electrodes must be held at clock “high” level during the process. If the register pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name	RØ1	RØ2	RØ3
E section transfer towards E output	E2	E1	E3
F section transfer towards F output	F2	F1	F3
G section transfer towards G output	G2	G1	G3
H section transfer towards H output	H2	H1	H3
E section transfer towards F output	E1	E2	E3
F section transfer towards E output	F1	F2	F3
G section transfer towards H output	G1	G2	G3
H section transfer towards G output	H1	H2	H3

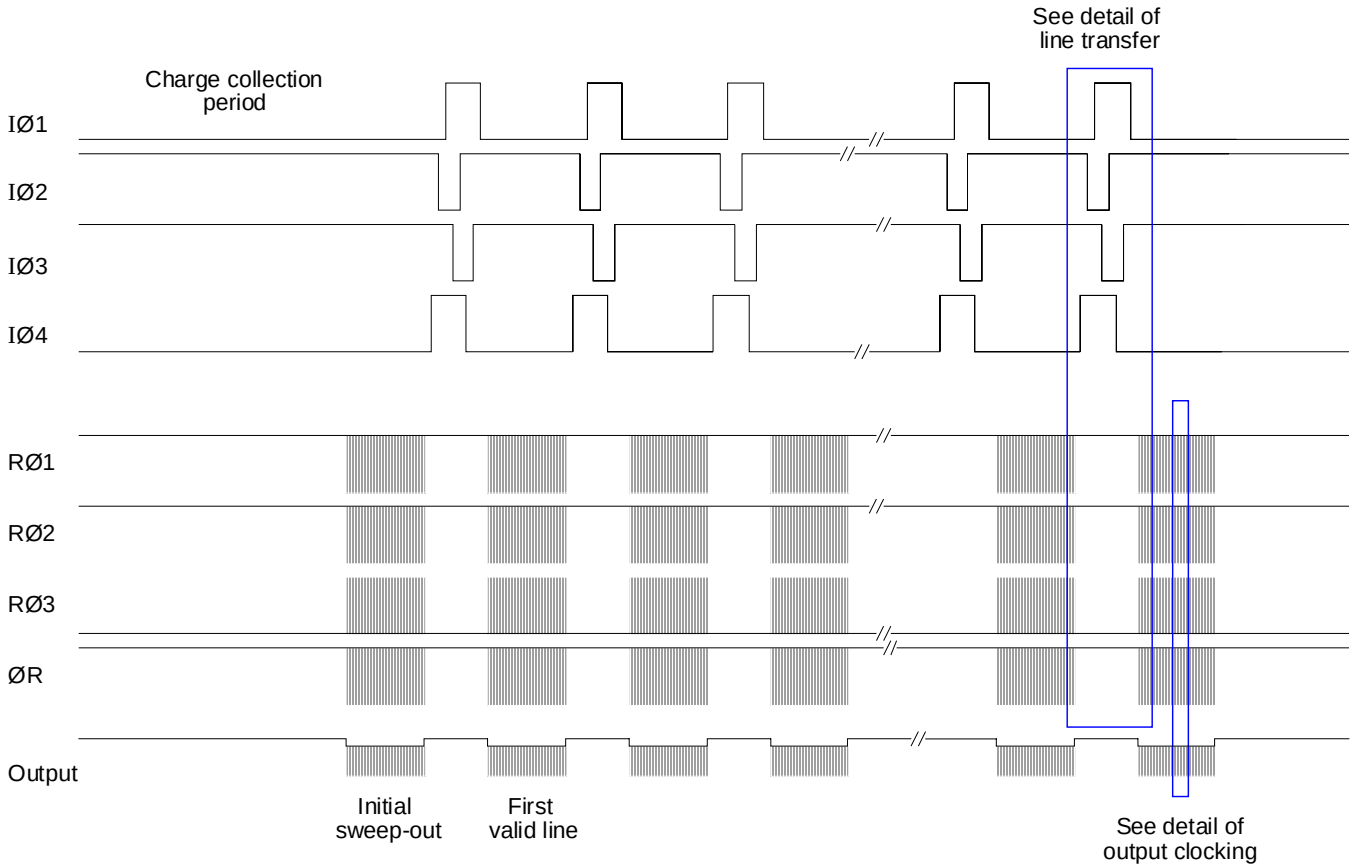
The first four sequences are for split register readout to all four outputs. The second four are for the reversal of direction in any half-section.

The last electrode before the output gate is separately connected to give the function of a summing well (SW). In normal readout (i.e. if not used for summing), SW is clocked as RØ3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

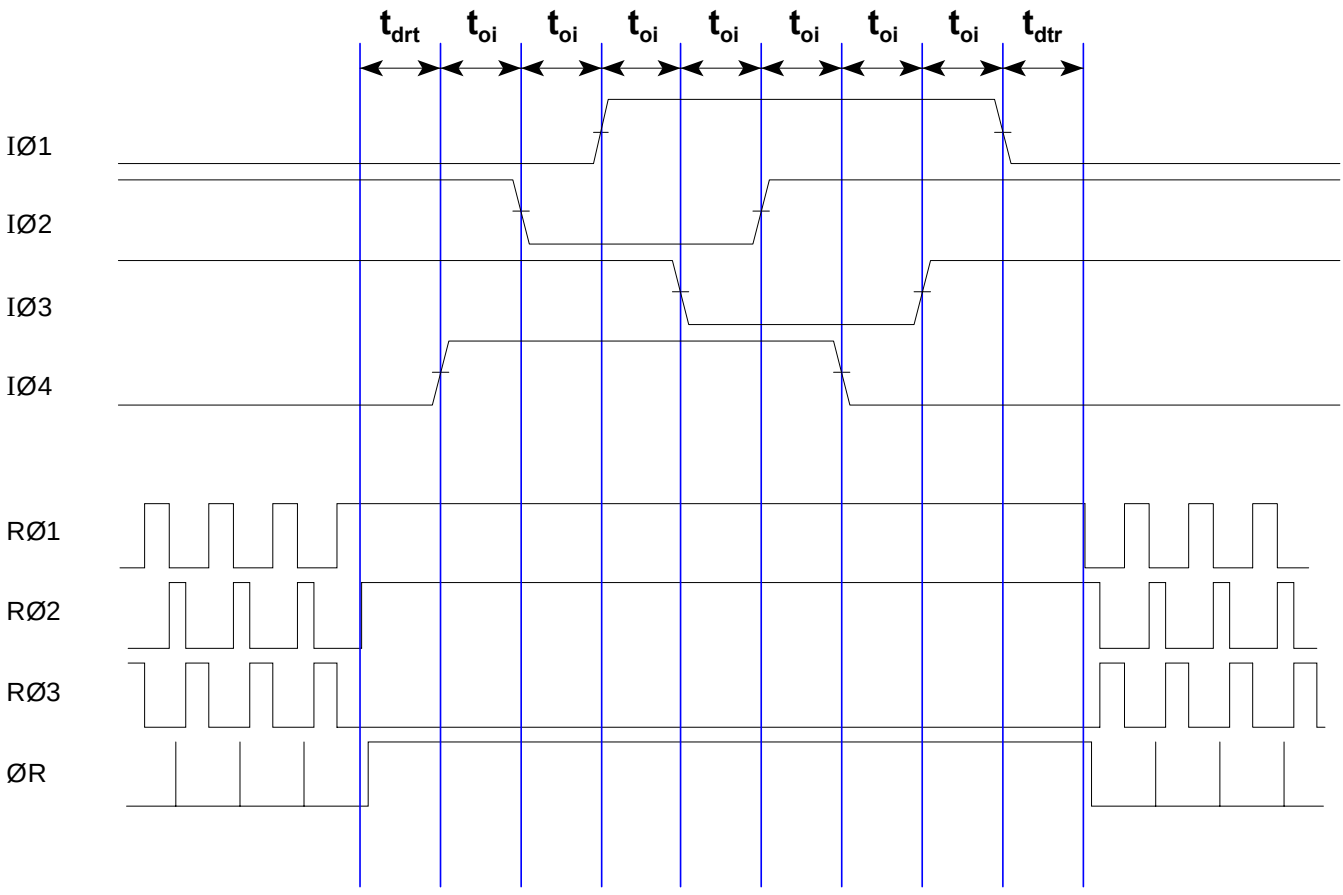
Alternatively, SW may be operated as a second output gate to provide the option of operation in low gain/high signal mode (mode 2) with OG high. If this mode of operation is used, then the sequencing of the output clocks must be changed, as charge will be transferred into the output node as RØ2 goes low (see notes 3 and9).

Image phases 2 and 3 should be held high during signal collection, as shown in the following figures.

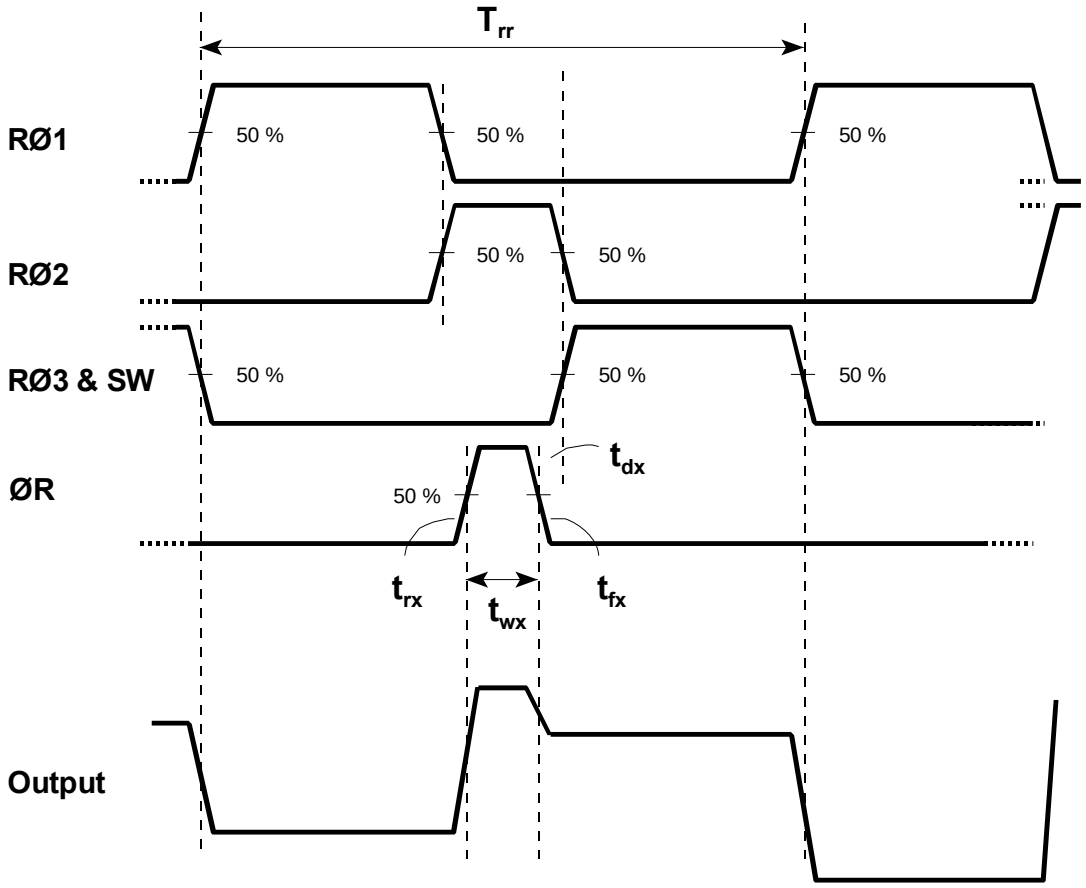
FRAME READOUT TIMING DIAGRAM

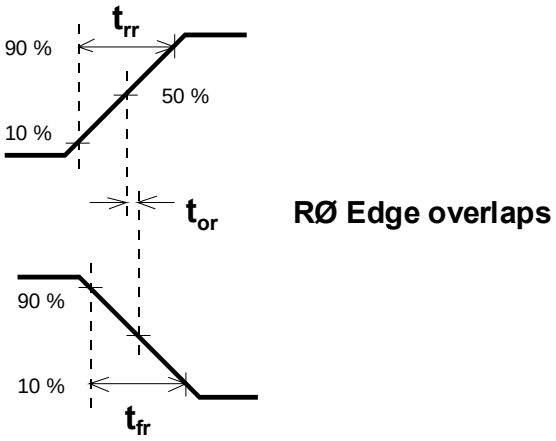


DETAIL OF LINE TRANSFER

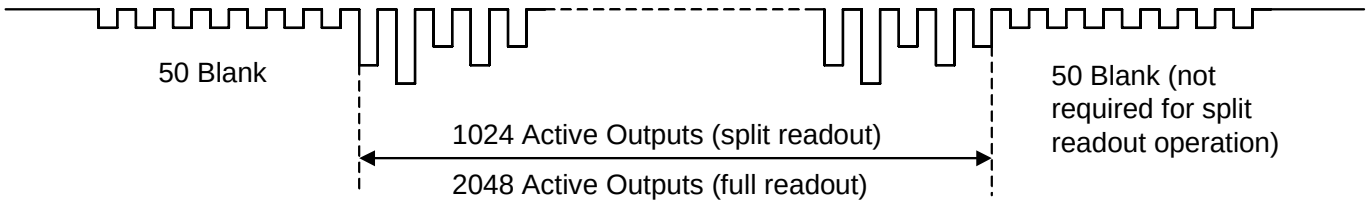


DETAIL OF OUTPUT CLOCKING (with SW clocked as RØ3)

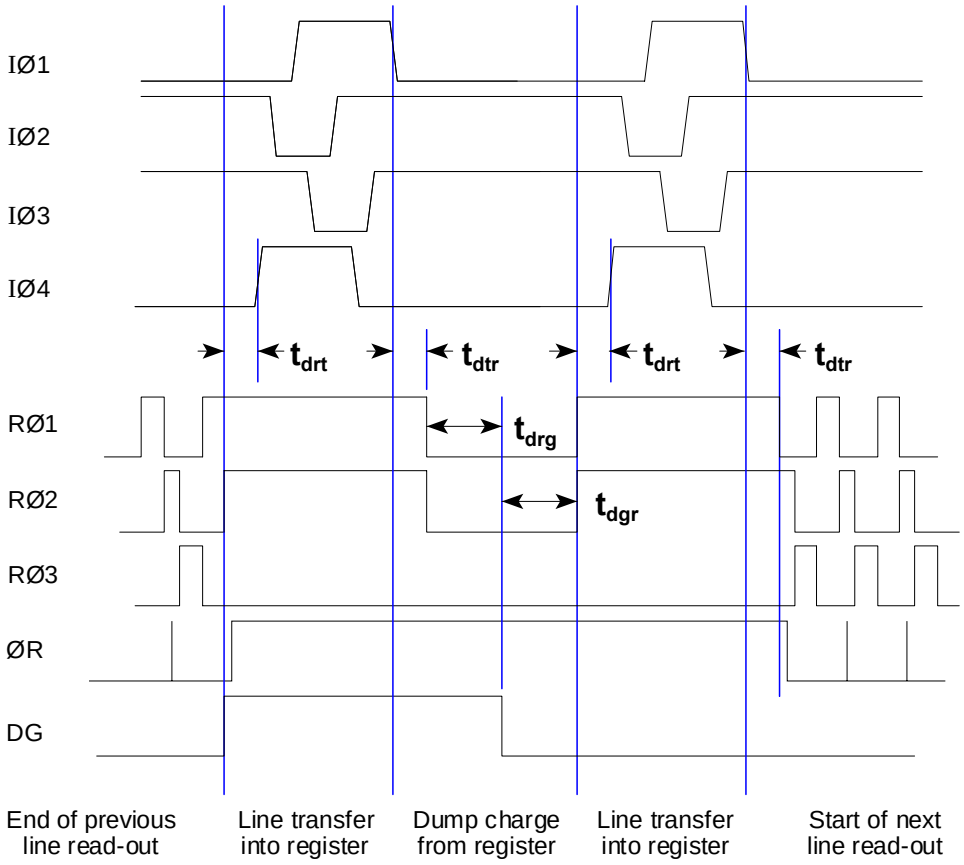




LINE OUTPUT FORMAT



DETAIL OF VERTICAL LINE TRANSFER (Single line dump)



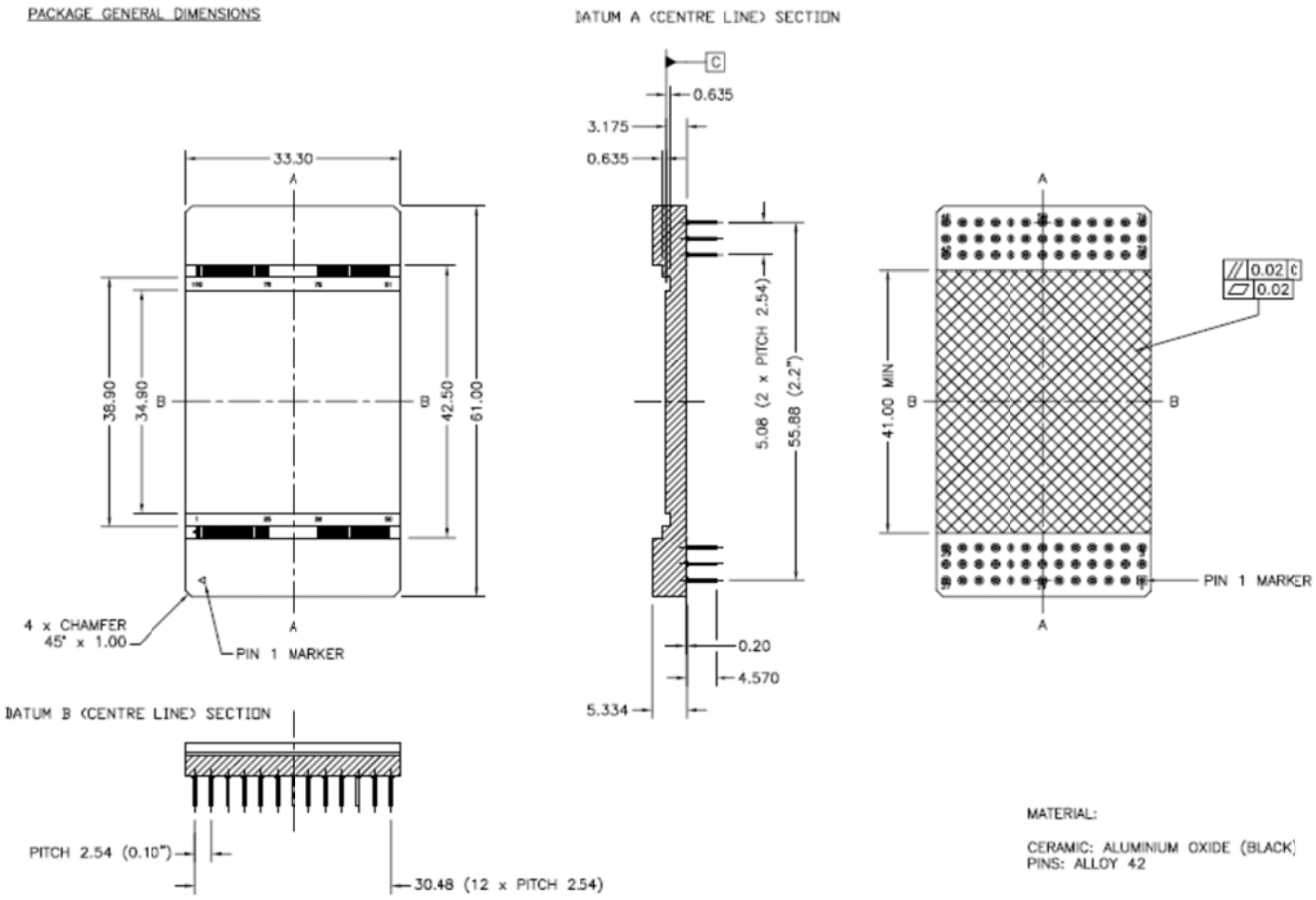
CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical (note 20)	Maximum	Units
T_i	Line transfer time (see note 16)	20	45	(see note 18)	µs
t_{oi}	Image clock pulse edge overlap	2	5	(see note 18)	µs
t_{ri}	Image clock and transfer gate pulse rise time	0.5	1	0.3 t_{oi}	µs
t_{fi}	Image clock pulse fall time	0.5	1	0.3 t_{oi}	µs
t_{drt}	Delay time, R∅ stop to I∅ rising	2	5	(see note 18)	µs
t_{dtr}	Delay time, I∅ falling to R∅ start	2	5	(see note 18)	µs
T_{rr}	Register clock period (see note 19)	330	1300	(see note 18)	ns
t_{drg}	Delay time, R∅ falling to DG rising (see note 11)	5	20	N/A	µs
t_{dgr}	Delay time, DG falling to R∅ rising (see note 11)	5	20	N/A	µs
t_{rr}	Register clock pulse rise time	10	50	(see note 18)	ns
T_{fr}	Register clock pulse fall time	10	50	(see note 18)	ns
t_{or}	Register clock pulse edge overlap	10	50	(see note 18)	ns
t_{wx}	Reset pulse width (see note 18)	>3 t_{rx}	150	(see note 18)	ns
t_{rx}	Reset pulse rise time	2	50	(see note 18)	ns
t_{fx}	Reset pulse fall time	2	50	(see note 18)	ns

NOTES

16. Generally $T_i = t_{drt} + 7t_{oi} + t_{dtr}$.
17. The R∅2 pulse-width is normally minimised, as shown, such that the R∅1 and R∅3 pulse widths can be increased to maximise the output reset (or reference) and signal sampling intervals.
18. As set by any system specifications.
19. The typical timing corresponds to values as used by e2v for factory tests at 750 kHz register frequency.
20. Devices are factory tested at values close to those shown in the “typical” column. In some cases these are merely a safe margin away from minimum times; in other cases they are determined by test camera considerations.

PACKAGE DETAIL



HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range 153 - 323 K

Storage temperature range 143 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 173 K.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures, thereby causing irreversible damage.

Maximum rate of heating or cooling: 5 K/min.